CT from the next driving stage. The controller **720** provides the second ground voltage VSS**2** to the first node Q in response to a switching signal output from the inverter **130**.

[0242] The controller **720** includes a first control transistor T**4**, a second control transistor T**9**, a third control transistor T**10**, and a capacitor Cb.

[0243] The first control transistor T**4** is connected between the input terminal IN and the first node Q, and includes a first control end and a second control end connected together with the input terminal IN.

[0244] The second control transistor T**9** is connected between the first node Q and the second ground terminal V**2**, and includes a first control end and a second control end connected together with the control terminal CT.

[0245] The third control transistor T**10** is connected between the first node Q and the second ground terminal V**2**, and includes a control end connected to a second node A.

[0246] The capacitor Cb is connected between the output terminal OUT and a control end of the controller **720** (e.g., the first node Q).

[0247] The inverter **130** outputs a switching signal to the second node A. The inverter **130** includes first to fourth inverter transistors T**12**, T**7**, T**13**, and T**8**.

[0248] The first inverter transistor T**12** includes an input end, a control end and an output end. The input end and the control end of the first inverter transistor T**12** are commonly connected to the clock terminal CK, and the output end of the first inverter transistor T**12** is connected to a control end of the second inverter transistor T**7**. The second inverter transistor T**7** includes an input end connected to the clock terminal CK, an output end connected to the second node A, and a control end connected to the output end of the first inverter transistor T**12**.

[0249] The third inverter transistor T**13** includes an output end connected to the output end of the first inverter transistor T**12**, a first control end connected to the carry terminal CR, a second control end connected to the bias voltage terminal VB, and an input end connected to the second ground terminal V**2**. The fourth inverter transistor T**8** includes an output end connected to the second node A, a first control end connected to the carry terminal CR, a second control end connected to the bias voltage terminal VB, and an input end connected to the second ground terminal V**2**. In an alternative exemplary embodiment, first control ends of the third and fourth inverter transistors T**13** and T**8** may be connected to the output terminal OUT.

[0250] The pull-down unit **740-1** includes a first pull-down transistor T**2**. The first pull-down transistor T**2** is connected between the output terminal OUT and the first ground terminal V**1**, and includes a control end connected to the control terminal CT.

[0251] The pull-down unit **740-2** includes a second pull-down transistor T**17**. The second pull-down transistor T**17** is connected between the carry terminal CR and the second ground terminal V**2**, and includes a control end connected to the control terminal CT.

[0252] The holding unit **750-1** includes a first holding transistor T**3**. The first holding transistor T**3** is connected between the output terminal OUT and the first ground terminal V**1**, and includes a control end connected to the second node A.

[0253] The holding unit **750-2** includes a second holding transistor T**11**. The second holding transistor T**11** is connected between the carry terminal CR and the first ground terminal V**1**, and includes a control end connected to the second node A.

[0254] Among transistors in the driving stage SRCi'**1** shown in FIG. **15**, the second output transistor T**15**, the first control transistor T**4**, the second control transistor T**9**, the third inverter transistor T**13** and the fourth inverter transistor T**8** are 4-terminal transistors, threshold voltages of which may be adjusted.

[0255] In such an embodiment, each of the second output transistor T**15**, the first control transistor T**4**, the second control transistor T**9**, the third inverter transistor T**13** and the fourth inverter transistor T**8** further includes the second control end in addition to the input end, the output end and the first control end.

[0256] In an exemplary embodiment shown in FIG. **15**, the second output transistor T**15**, the first control transistor T**4**, the second control transistor T**9**, the third inverter transistor T**13** and the fourth inverter transistor T**8** are 4-terminal transistors, but not being limited thereto. In an alternative exemplary embodiment, at least one of the second output transistor T**15**, the first control transistor T**4**, the second control transistor T**9** and the fourth inverter transistor T**8** may not be a 4-terminal transistor.

[0257] A structure and a threshold voltage change of the 4-terminal transistors are the same as those described above with reference to FIG. **6** and FIG. **7**, and any repetitive detailed description thereof will be omitted.

[0258] FIG. **16** is a timing diagram of signals of a display device according to an alternative exemplary embodiment.

[0259] As shown in FIG. **16**, a first clock signal CKV and a second clock signal CKVB may be signals having phases inverted from each other. The first clock signal CKV and the second clock signal CKVB may have a phase difference of about 180°. The first clock signal CKV and the second clock signal CKVB respectively have a low level VL-C, a voltage level of which is low, and a high level VH-C, a voltage level of which is relatively high. The high level VH-C may have a voltage level of about 10 V. The low level VL-C may have a voltage level of about −14 V. The low level VL-C may have the same voltage level as the second ground voltage VSS**2**.

[0260] One frame period includes a period, during which a voltage level of an i-th gate signal G[i] is the low level VL-G, and a period, during which a voltage level of the i-th gate signal G[i] is the relatively high level VH-G. The low level VL-G of the i-th gate signal G[i] may be the same voltage level as the first ground voltage VSS**1**. The low level VL-G may be about −12 V.

[0261] During some periods, the i-th gate signal G[i] may have the same voltage level as the low level VL-C of the first clock signal CKV or the second clock signal CKVB. A low level VL-C of the first clock signal CKV or the second clock signal CKVB is output by a pre-charged first node Q before the i-th gate signal G[i] reaches the high level VH-G.

[0262] The high level VH-G of the i-th gate signal G[i] may have the same level as the high level VH-C of the first clock signal CKV or the second clock signal CKVB.

[0263] The i-th carry signal CR[i] may have the low level VL-C having a low voltage level and the high level VH-C having a relatively high voltage level. Since the i-th carry signal CR[i] is generated based on the first clock signal CKV, the i-th carry signal CR[i] has a voltage level that is the same as or similar to the first clock signal CKV.